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09/411,418	10/01/1999	JOHN A. CAREY	99-TK-257	8281

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

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17

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/411,418	CAREY, JOHN A.	
	Examiner	Art Unit	
	Heng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicant's Amendment and Response (paper # 12) to Office Action dated January 29, 2004 (paper # 11), mailed March 29, 2004.

1-1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

1-2. Claim 3 has been amended; claims 1-20 and 25 are pending.

1-3. Claims 1-20 and 25 have been examined and rejected.

1-4. The indicated allowability of claims 3 and 4 is withdrawn because Applicant has amended claim 3. Rejections based on the previously cited reference to McGeer et al., U.S. Patent 6,421,808 issued July 16, 2002, follow.

Drawings

2. The proposed drawing correction to FIG. 4 cont. was received on March 29, 2004. The replacement drawing is acceptable. The objection to the drawings has been withdrawn.

Specification

3. Applicant has amended the specification. The objections to specification in section 5 of paper # 11 have been withdrawn.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-4, 13-20, and 25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

5-1. For example, as described in [0049] lines 1-2 of the substitute specification, "Embodiments of the present invention can be implemented in systems where the requests and responses are not in a packet format". In other words, there are no limitations on the requests and responses. However, in the rest of the specification Applicant teaches implementations in systems where the requests and responses are only in a packet format. In the independent claims 1, 3, 13, 17, and 25, Applicant has only amended the "requests" to "packet-format requests". There is no amendment to "responses". Accordingly, without undue experimentation, it is unclear how one skilled in the art may implement the invention in systems where the "responses" are not in a packet format, but in, for example, a free format.

5-2. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2, 4, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7-1. Dependent claim 2 recites the limitation "said number of requests which are permitted to be outstanding are defined if the interconnect is responsible for ordering" in lines 1-3 of the claim. There is insufficient antecedent basis for this limitation in the claim if the initiator is defined to be responsible for ordering responses in claim 1. On the other hand, if the interconnect is defined to be responsible for ordering responses in claim 1, the above-mentioned limitation is redundant because said step has already been recited in claim 1.

7-2. Dependent claim 4 recites the limitation "said the step of defining the maximum number of possible outstanding requests is performed only if the interconnect is responsible for ordering the responses" in lines 1-3 of the claim. There is insufficient antecedent basis for this limitation in the claim if the target is defined to be responsible for ordering responses in claim 3. On the other hand, if the interconnect is defined to be responsible for ordering responses in claim 3, the above-mentioned limitation is redundant because said step has already been recited in claim 3.

7-3. Claim 19 recites the limitation "said the maximum number of outstanding request" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 19 also recites the limitation "said queue" in line 2 of the claim. It is vague and indefinite about "said queue" because both claim 17 recites "a queue" in line 6 and claim 18 recites "access queue" in line 2.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8-1. Claims 1-20 and 25 are rejected under 35 U.S.C. 101 because the inventions as disclosed in claims are directed to non-statutory subject matter. In other words, claims 1-20 and 25 claim a method or a model that does nothing more than manipulating program parameters and is not in the technology arts.

8-2. The Examiner acknowledges that even though the claims are presently considered non-statutory they are additionally rejected below over the prior art. The Examiner assumes the Applicants will amend the claims to overcome the 101 rejections and thus make the claims statutory.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9-1. Claims 1-20 and 25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-32 of U.S. Patent No. 6,460,174. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are all directed to designing an integrated circuit comprising initiator and target connected by an interconnect.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

11. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by McGeer et al., U.S. Patent 6,421,808 issued July 16, 2002, and filed April 22, 1999.

11-1. Regarding claim 1, McGeer et al. disclose a method for designing an initiator in an integrated circuit, said initiator being connected to an interconnect and arranged to issue packet-format requests, said method comprising the steps of:

defining if the interconnect is to be responsible for ordering responses to packet-format requests issued by said initiator (defining the responsibility of ordering responses in a packet-format network is inherent for designing network);

defining the maximum number of requests which are permitted to be outstanding at the same time (a specific number of FIFO entries, column 19, lines 11-13; providing sufficient buffer space at the reassembly point in a packet-format network is inherent for designing network); and

defining if a delay stage is required in said initiator (defining the variable is a latch or a wire, column 31, lines 26-30).

11-2. Regarding claim 2, McGeer et al. further disclose said number of requests which are permitted to be outstanding are defined if the interconnect is responsible for ordering (a specific number of FIFO entries, column 19, lines 11-13).

11-3. Regarding claim 3, McGeer et al. disclose a method for designing a target in an integrated circuit, said target being connected to an interconnect and arranged to generate responses to packet-format requests, the method comprising the steps of:

defining if the target or the interconnect is responsible for ordering responses (defining the responsibility of ordering responses in a packet-format network is inherent for designing network);

defining the maximum number of possible outstanding requests which can be supported by said target (a specific number of FIFO entries, column 19, lines 11-13; providing sufficient buffer space at the reassembly point in a packet-format network is inherent for designing network); and

defining if a delay stage is required in said target (defining the variable is a latch or a wire, column 31, lines 26-30).

11-4. Regarding claim 4, McGeer et al. further disclose said the step of defining the maximum number of possible outstanding requests is performed only if the interconnect is responsible for ordering the responses (a specific number of FIFO entries, column 19, lines 11-13).

11-5. Regarding claim 5, McGeer et al. disclose a method for designing an interconnect having routing resources, said interconnect arranged to allow initiators to send packet-format requests to targets (channels, column 13, lines 20-31), said method comprising the steps of defining:

the number of routing resources between the initiator and the target (user defined channels, column 16, lines 60-67);

the arbitration method for arbitrating between requests (channel arbiter, column 17, lines 16-58); and

the association between the routing resources and the targets (receiver interface, column 17, lines 59-63).

11-6. Regarding claim 6, McGeer et al. further disclose said method further comprises the step of determining if a delay is required after arbitration (defining the variable is a latch or a wire, column 31, lines 26-30).

11-7. Regarding claim 7, McGeer et al. disclose a method for designing an interconnect having routing resources, said interconnect arranged to allow targets to send packet-format responses to initiators in response to packet-format requests from initiators, said method comprising the steps of defining:

the number of routing resources between the target and the initiator (user defined channels, column 16, lines 60-67);

the arbitration method for arbitration between responses (channel arbiter, column 17, lines 16-58); and

the association between the routing resources and the initiator(sender interface, column 17, lines 59-63).

11-8. Regarding claim 8, McGeer et al. further disclose said method further comprises the step of determining if a delay is required after arbitration (defining the variable is a latch or a wire, column 31, lines 26-30).

11-9. Regarding claim 9, McGeer et al. disclose a method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said initiators and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled (defining the responsibility of ordering responses in a packet-format network is inherent for designing network), and selecting one of the plurality of

arbitration methods available in said model (channel arbiter, column 17, lines 16-58; priority decoder, column 12, lines 25-29).

11-10. Regarding claim 10, McGeer et al. disclose a method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said initiators and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled (defining the responsibility of ordering responses in a packet-format network is inherent for designing network), and selecting one of the plurality of arbitration methods available in said model (channel arbiter, column 17, lines 16-58; priority decoder, column 12, lines 25-29), wherein the method further comprises selecting if a delay is to be provided after arbitration has been performed (defining the variable is a latch or a wire, column 31, lines 26-30).

11-11. Regarding claim 11, McGeer et al. disclose a method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said targets and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled (defining the responsibility of ordering responses in a packet-format network is inherent for designing network), and selecting one of the plurality of

arbitration methods available in said model (channel arbiter, column 17, lines 16-58; priority decoder, column 12, lines 25-29).

11-12. Regarding claim 12, McGeer et al. disclose a method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said targets and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled (defining the responsibility of ordering responses in a packet-format network is inherent for designing network), and selecting one of the plurality of arbitration methods available in said model (channel arbiter, column 17, lines 16-58; priority decoder, column 12, lines 25-29), wherein the method further comprises selecting if a delay is to be provided after arbitration has been performed (defining the variable is a latch or a wire, column 31, lines 26-30).

11-13. Regarding claim 13, McGeer et al. disclose a model of an initiator to be used in designing an integrated circuit in which an initiator is arranged to send packet-format requests to one or more targets via an interconnect, said model comprising:

an address decode stage for identifying the target for which a given message is intended (determining the default channel, column 13, lines 33-67); and

a dependency stage for determining the allowability of a request, the operation of said dependency stage being selectable (safe channel, column 14, lines 10-37), said dependency stage being such that the model supports an arrangement where the interconnect is responsible for

maintaining the order of responses from a target to the requests (stored in a FIFO resides in the channel, column 13, lines 59-65).

11-14. Regarding claim 14, McGeer et al. further disclose a retime stage is provided in said model, the retime stage arranged to provide a delay or no delay (defining the variable is a latch or a wire, column 31, lines 26-30).

11-15. Regarding claim 15, McGeer et al. further disclose an access queue is provided for storing requests for which responses have not been received (stored in a FIFO resides in the channel, column 13, lines 59-65).

11-16. Regarding claim 16, McGeer et al. further disclose the maximum number of requests which can be stored in the queue is definable (a specific number of FIFO entries, column 19, lines 11-13).

11-17. Regarding claim 17, McGeer et al. disclose a model of a target to be used in designing an integrated circuit in which one or more initiators are arranged to send packet-format requests to a target and the target is arranged to send responses to the requests via an interconnect, said model comprising:

a locking stage which permits locked transactions to occur if required (blocks itself, column 14, lines 33-36); and

a decode state which decodes information stored in a queue into an address for the response (decoding the address, column 49, lines 1-30).

11-18. Regarding claim 18, McGeer et al. further disclose said model comprises an access queue which store information on the requests received by the target (shadow registers, column 14, lines 21-63).

11-19. Regarding claim 19, McGeer et al. further disclose the maximum number of outstanding request which can be stored in said queue is definable (a set of auxiliary latches are allocated, column 14, lines 24-26).

11-20. Regarding claim 20, McGeer et al. further disclose said queue is in the initiator (shadow registers, column 14, lines 21-63).

11-21. Regarding claim 25, McGeer et al. disclose a method for designing an initiator in an integrated circuit, said initiator being connected to an interconnect and arranged to issue packet-format requests, said method comprising the steps of:

defining if the interconnect is to be responsible for ordering responses to requests issued by said initiator (defining the responsibility of ordering responses in a packet-format network is inherent for designing network); and

defining if a delay stage is required in said initiator (defining the variable is a latch or a wire, column 31, lines 26-30).

Applicant's Arguments

12. Applicant argues the following:

(1) "Finality of the January 29, 2004 Office Action is premature" (page 10, paper # 12).

(2) "The amendment to claims 3-4 is believed to overcome the rejection" (page 11, paragraph 1, paper # 12).

(3) "McGeer's invoking port cannot take responsibility for delivering a message" (page 11, paragraph 4, paper # 12).

(4) "there is no 'delay' described in the McGeer and so the claimed step of defining if a delay state is required is not shown or fairly suggested" (page 11, last paragraph, paper # 12).

(5) "As noted at column 17, lines 20-21, a port can take messages only from one channel. With this restriction there would be little purpose in McGeer having a step of defining the number of routing resources as that number is restricted to be one" (page 12, paragraph 4, paper # 12).

(6) "it appears that McGeer's arbiter has only one arbitration method, not a plurality as claimed for in claim 12" (page 13, paragraph 1, paper # 12).

(7) "As noted above, McGeer shows a system in which the initiator can not take responsibility for ordering responses" (page 13, paragraph 2, paper # 12).

(8) "the 'shadow registers' cited in the Office Action refer to a structure defined in the initiator, not the target" (page 13, paragraph 3, paper # 12).

Response to Arguments

13. Applicant's arguments have been fully considered.

13-1. Applicant's argument (1) is persuasive. The finality of the January 29, 2004, Office Action has been withdrawn as indicated in section **1-1** above.

13-2. Applicant's argument (2) is not persuasive. The claimed "responses" have no support because only "packet-format responses" have been taught in the specification. Claims 1-4, 13-20, and 25 are rejected under 35 U.S.C. 112, first paragraph, as detailed in sections **5-1** to **5-2** above.

13-3. Applicant's arguments (3) and (7) are not persuasive. For example, McGeer et al. disclose, "the order among bytes in the same packet should be maintained by the masters" in column 47, lines 36-37. In other words, the example of the InfoPad project has the data source to maintain the ordering.

13-4. Applicant's argument (4) is not persuasive. For example, McGeer et al. disclose in column 31, lines 28-30, "If the variable is a latch, the new value will be effective in the next clock cycle. If the variable is a wire, then the effect will be visible immediately". In other words, delay or not can be defined by determining the type of a variable.

13-5. Applicant's argument (5) is not persuasive. Claim 5 recites the limitation of defining "the number of routing resources between the initiator and the target". Defining "the number of routing resources" to be more than one has not been claimed. The "user defined channels" disclosed by McGeer et al. meet the claimed limitation.

13-6. Applicant's argument (6) is not persuasive. For example, McGeer et al. disclose in column 25, lines 7-23, "The channel uses a round robin scheme to schedule multiple requests". In other words, McGeer et al. do disclose a second arbitration method.

13-7. Applicant's argument (8) is not persuasive. A queue recited in claims 17-18 refers to a structure defined in the target has not been explicitly claimed.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
June 1, 2004

Thai Phan
Patent Examiner
AU: 2128